In the Claims:

Please amend the claims as follows:

1. (Canceled)

2. (Currently Amended) A programmable jitter signal generator as defined in Claim ~~1~~ 4 wherein the delay unit comprises a delay chain.

3. (Currently Amended) A programmable jitter signal generator as defined in Claim ~~1~~ 4 wherein the selection unit comprises a multiplexer.

4. (Currently Amended) A programmable jitter signal generator comprising:

a jitter distribution control unit;

a selection unit in signal communication with the jitter distribution control unit; and

a delay unit in signal communication with the selection unit;

~~A programmable jitter signal generator as defined in Claim 1,~~ the jitter distribution control unit comprising:

a binary counter;

a random access memory in signal communication with the binary counter; and

a random number generator in signal communication with the random access memory.

5. (Original) A programmable jitter signal generator as defined in Claim 4 wherein the jitter distribution control unit provides the greatest flexibility to control timing jitter.

6. (Currently Amended) A programmable jitter signal generator comprising:

a jitter distribution control unit;

a selection unit in signal communication with the jitter distribution control unit; and

a delay unit in signal communication with the selection unit,

~~A programmable jitter signal generator as defined in Claim 1,~~ the jitter distribution control unit comprising:

a plurality of flip-flop devices;

at least one summing device having one input coupled to the output of a first flip-flop device, and an output coupled to the input of a second flip-flop device; and

at least one gain device having an output coupled to a second input of the at least one flip-flop device.

7. (Original) A programmable jitter signal generator as defined in Claim 6, the jitter distribution control unit comprising a plurality of linear feedback shift registers ("LFSR").

8. (Original) A programmable jitter signal generator as defined in Claim 7 wherein all random patterns can be deduced from an LFSR seed to simplify the design.

9. (Currently Amended) A programmable jitter signal generator as defined in Claim ~~1~~ 4, the delay unit comprising a modified delay chain having at least one inverter coupled to the output of a delay chain.

10. (Currently Amended) A programmable jitter signal generator as defined in Claim ~~1~~ 4, the delay unit comprising a modified delay chain having at least one logical gate coupled to the input of a delay chain.

11. (Canceled)

12. (Currently Amended) A method as defined in Claim ~~11~~ 17 wherein:

each multiple of the base time increment corresponds to one of a plurality of delay cells; and

the delayed reference signal is selected by selecting a delay cell corresponding to the programmed delay of the output.

13. (Currently Amended) A method as defined in Claim ~~11~~ 17 wherein delaying the reference signal comprises adjusting the time instants of the rising edge of the received reference signal.

14. (Currently Amended) A method as defined in Claim ~~11~~17, further comprising controlling the jitter distribution of an output signal in accordance with the programmed control unit.

15. (Currently Amended) A method as defined in Claim ~~11~~17, further comprising controlling the average jitter magnitude of an output signal in accordance with the programmed control unit.

16. (Currently Amended) A method as defined in Claim ~~11~~17 wherein selecting the delayed reference signal comprises multiplexing the delayed reference signal from one of a plurality of delay cells in accordance with the output of the programmed control unit.

17. (Currently Amended) A method of generating a programmable jitter signal, the method comprising:

programming a control unit;

receiving a reference signal;

delaying the received reference signal by a multiple of a base time increment; and

selecting a delayed reference signal delayed by a desired multiple of the base time increment in accordance with the programmed control unit,

~~A method as defined in Claim 11~~ wherein programming the control unit comprises:

initializing a binary counter;

generating a random number in correspondence with the binary counter; and

storing the generated ~~binary~~ random number for later retrieval.

18. (Currently Amended) A method of generating a programmable jitter signal, the method comprising:

programming a control unit;

receiving a reference signal;

delaying the received reference signal by a multiple of a base time increment; and

selecting a delayed reference signal delayed by a desired multiple of the base time increment in accordance with the programmed control unit,

~~A method as defined in Claim 11~~ wherein programming the control unit comprises:

providing a plurality of flip-flop devices;

providing at least one summing device having one input coupled to the output of a first flip-flop device, and an output coupled to the input of a second flip-flop device;

providing at least one gain device having an output coupled to a second input of the at least one flip-flop device; and

assigning the gain of the at least one gain device.

19. (Original) A method as defined in Claim 18, further comprising arranging the provided flip-flop, summing and gain devices to operate as linear feedback shift registers ("LFSR").

20. (Original) A method as defined in Claim 18, further comprising deducing generated random jitter patterns from an LFSR seed.

21. (Currently Amended) A method as defined in Claim ~~11~~17, further comprising inverting the output of a delay chain.